

Application Information

Application number:: 09/697,305

Filing Date:: 10/27/00

Application Type:: Regular

Subject Matter:: Utility

Suggested Classification::

Suggested Group Art Unit:: 2133

CD-ROM or CD-R?:: None

Number of CD disks:: None

Number of copies of CDs:: None

Sequence submission::

Computer Readable Form (CRF):: No

Number of copies of CRF:: None

Title:: FAULT DETECTING METHOD AND

LAYOUT METHOD FOR SEMICONDUCTOR

INTEGRATED CIRCUIT

Attorney Docket Number:: YMOR:186

Request for Early Publication:: No

Request for Non-Publication:: No

Suggested Drawing Figure:: 1

Total Drawing Sheets:: 50

Small Entity:: No

Latin Name::

Variety denomination name::

Petition included:: No

Petition Type:: None

Licensed US Govt. Agency:: None

Contract or Grant Numbers:: None

Secrecy Order in Parent Appln. ?:: No

Applicant Information

Applicant Authority Type:: Inventor

Primary Citizenship

Country:: Japan

Status:: Full Capacity

Given Name:: Takaki

Middle Name::

Family Name:: Yoshida

Name Suffix::

City of Residence:: Ibaraki-shi

State or Province of

Residence:: Osaka

Country of Residence:: Japan

Street of mailing address:: c/o Matsushita Electric Ind.

Co., Ltd., 1006, Oaza Kadoma

City of mailing address:: Kadoma-shi

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Given Name::

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Shimoda

Name Suffix::

City of Residence::

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Postal or Zip Code of

mailing address::

571-8501

Correspondence Information

Correspondence Customer Number::

6160

Representative Information

Representative Customer Number::

6160

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application			

Foreign Priority Information

Country::	Application number::	Filing Date::	Priority Claimed::
Japan	11-307872	10/29/99	Yes

Assignee Information

Assignee name:: Matsushita Electric Industrial

Co., Ltd.

Street of mailing address:: 1006, Oaza Kodoma

City of mailing address:: Kadoma-shi

State or Province of

mailing address:: Osaka

Country of mailing address:: Japan

Postal or Zip Code of

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